3D Resist Profile Full Chip Verification and Hot Spot Disposition

Qing Yang*[a], ShyueFong Quek[a], YeeMei Foong[a], Jens Hassmann[b], DongQing Zhang[a], Andre Leschok[b],Tang Yun[a];
Mu Feng[c], Stanislas Baron[c], JianHong Qiu[c], Taksh Pandey[c]; Bo Yan[c], Russell Dover[c]

[a]GLOBALFOUNDRIES, 60 Woodlands Industrial Park D Street 2, Singapore, 738406
[b]GLOBALFOUNDRIES, 101 Wilschdorfer Landstr, Dresden, German, 01109
[c]ASML Brion Technologies, 4211 Burton DR., Santa Clara, CA, 95054, USA

ABSTRACT

For 28 nm technology node and below resist profiles need to be taken in to consideration during optical proximity correction (OPC) and verification. The low k_1 results in a shallower depth of focus and thus thinner resists, which combined with the process limits increases the risk of resist degradation. Only considering the resist critical dimensions at a single focal plane (such as at the bottom of the resist stack) will miss the impact of the resist 3D profile, like top loss or bottom footing, which can transfer to etch hard pattern failures. To date, modeling to study resist 3D profiles has been available using rigorous simulators and has been used as a verification method for hot spots captured during full chip OPC verification, but not for full chip verification due to the high computational run time cost.

This paper demonstrates a 3D resist compact OPC model concept and implementation in a full chip OPC and verification flow. The results show significant improvement for full chip OPC quality with a good correlation between simulation and real wafer hot spots.

Because resist profiles are not directly correlated to etch failure, the relationship between the resist profile and etch failures and how to characterize the threshold to dispose the hot spots for the 3D compact model was also investigated.

Keywords: OPC, 3D resist modeling, resist top loss, etch failure

1. INTRODUCTION

For 28 nm tech node with given k1 below 0.3, the lithography process tends to dictate the process margin for production. This paper focuses on a 28 nm node with a minimum pitch of 90 nm, a 45 nm line width and with 45 nm spacing. A 45 nm dimension is almost the minimum dimension that can be resolved with single exposure using a hyper-NA immersion scanner. With this patterning difficulty the resist process is usually optimized to improve the process window margin by using thinner resist to have a high contrast, but which has a side effect with etch selectivity. With thin, high contrast resist etch selectivity becomes worse. The thin metal hard mask (TMHM) used in a 'trench first metal hard mask' (TFMHM) process can be eroded during the TMHM etch process, even though the TFMHM process uses the hard mask to etch the low-k material. In addition this eroded hard mark in the previous etch step can be etched into the low-k material to define the metal space for the metal line insulation during the etching process of the low-k material. The main factors, which determine the quality of the lithography process to the proceeding modules of integration flow, like Etch and CMP processes, are photoresist height and the resist slope after develop.

Optical Microlithography XXVI, edited by Will Conley, Proc. of SPIE Vol. 8683, 86831N

For such a low k1 factor tech node, OPC is a key factor to enable a manufacturable process. Typical OPC compact models are calibrated at a single image depth (usually at the bottom of the resist stack) with corresponding CD measurement. As such the OPC correction and verification are targeted at a single optical plane. However resist profiles are almost never strictly perpendicular to the wafer plane and always have some side angle. For advanced technology nodes the resist thickness has become so thin that resist loss can be a dominant factor leading to etch failure. Resist profiles are not only a resist material characteristic but also depends on optical effects, including local design layouts. As such for different structures within the same mask the resist profile can vary significantly resulting in localized hotspots.

For OPC correction to meet the design intent there are many options to achieve the final corrected layout. With a standard OPC compact model wafer measurements are taken at a single resist plane and model calibration is not difficult. However the OPC is unaware of the resist profile during correction and cannot meet the target of another resist plane. As such it is probable that some corrected layouts have a bad resist profile while meeting the target at the single resist plane. Consequently conventional full chip verification using a single image depth compact OPC model, to detect hot spots, is not sufficient to meet the technology challenge introduced by varying resist profiles.

Rigorous simulation tools like Prolith™ and S-Litho™ can predict 3D resist profiles, but are limited to simulation or verification of small layout clips due to the high computational run time cost. Figure 1 shows an example of rigorous simulation of a hotspot that has localized resist top loss. A compact OPC model which has awareness of the 3D resist information is needed for full chip verification. For layers with complex layouts and challenging process windows, such as early metal layers, 3D resist full chip verification becomes more and more important.

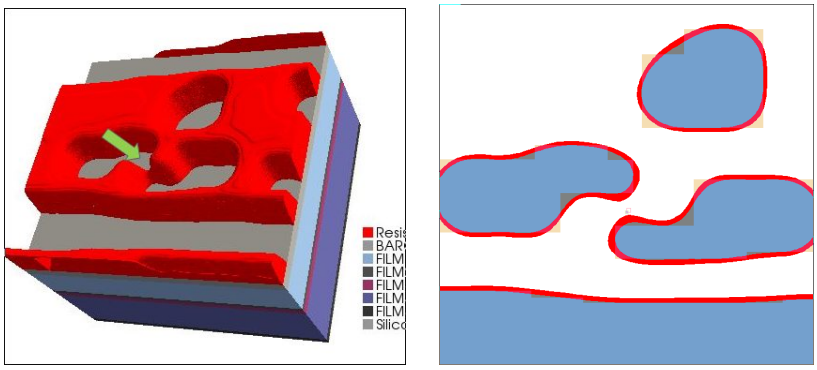

Figure 1. a) Rigorous simulation of a localized resist top loss hotspot; b) A planar view of the resist contour simulation of the same hotspot showing the resist contour at the bottom and top of the resist stack. The width of the red lines indicates a greater resist profile slope from bottom to top.

2. Methodology

A fast 3D resist compact OPC model was developed with Brion Technologies to perform full chip verification. In this 3D resist compact model the resist profile factor is taken into account only in the optical part of the model. Atomic force microscopy (AFM) data, for focus sensitive structures, was collected at nominal and focus exposure matrix (FEM) conditions and used to verify the model behavior through the process window. Top SEM images of etch profiles for some 2D structure were also used to verify the model, as the etch profile correlates to the resist profile in many respects. Figure 2a illustrates an example of post etch SEM and the simulated resist contours using the new OPC model. Finally rigorous model simulation and the 3D resist compact OPC model simulation contours were compared to each other in Figure 2b, as well.

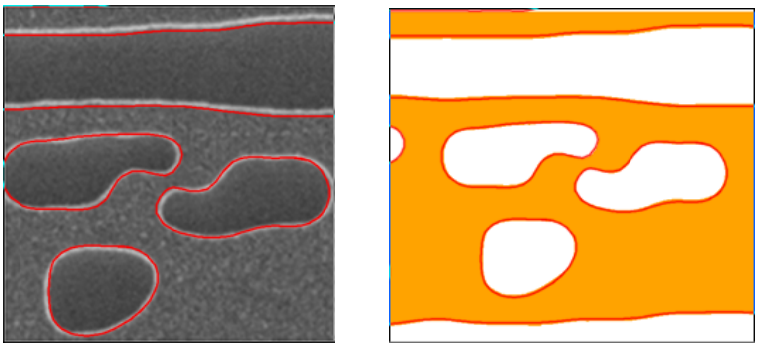

Figure 2 a) Post etch SEM image overlap with 3D compact model simulation contour; b) 3D rigorous model simulation contour overlap with 3D compact OPC model simulation contour in same site.

Across a full chip layout different features have different resist profiles and different resist thickness, resulting in significant resist top loss in some cases. With a 3D resist compact model it is necessary to correlate the etch failure with resist top loss and identify how to disposition these hot spots captured by full chip verification. Etch wafers were used to determine the minimum resist thickness needed to meet the etch requirements for certain pattern shapes to avoid post CMP failure and CD variation. Figure 3 and Figure 4 show the comparison of two different OPC layouts with the nominal resist model simulation contour and 3D compact model simulation contour. A detected hard bridge, found with the 3D resist compact model is shown in Figure 3a, which correlated well with the etched wafer results, showing that this hypothesis was well correlated. Figure 3b shows the same area and contours after using OPC based on the 3D resist compact model, to ensure a safer etch process.

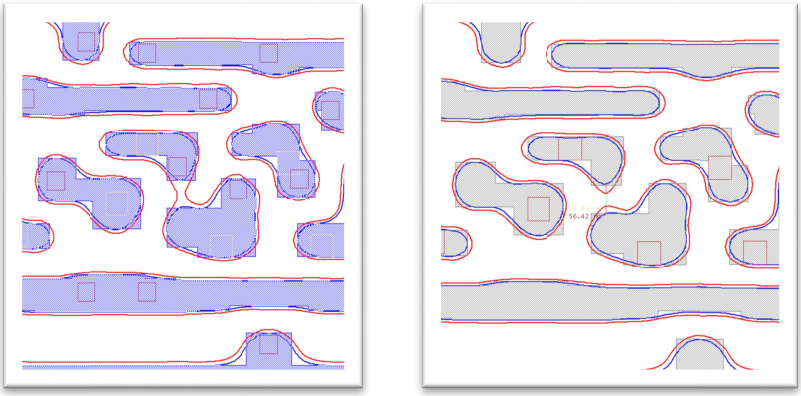

Figure 3 a) Nominal resist model simulation contour and 3D compact model simulation contour overlap shows discrepancy of bottom and top resist behavior; b) Nominal resist model simulation contour and 3D compact model simulation contour overlap shows a more robust OPC solution provides better top resist profile while not scarifying bottom CD target.

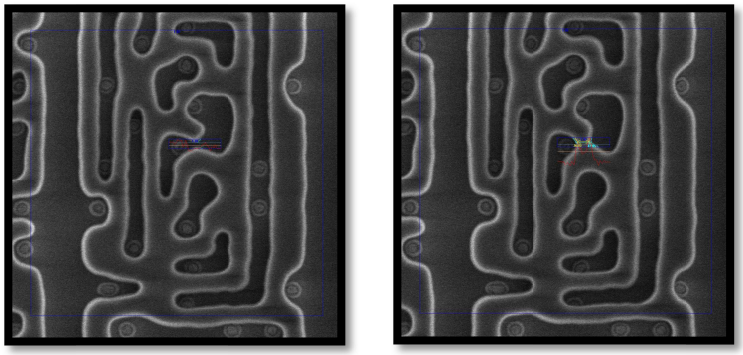

Figure 4 a) Top down SEM image of post etch wafer at same location in Figure 3a which shows a hard metal short that correlates well to the 3D resist compact model prediction; b) Top down SEM image of post etch wafer at the same location as in Figure 3b which shows an etch profile improvement when the OPC used the 3D resist compact model.

Every model has an extrapolation boundary. Near the boundary the simulated values have less accuracy compared to the rest of the model. This 3D compact resist OPC model also has such a limitation in that it cannot be used to exactly predict the exact plane where the resist coverage ends. This means that a specific resist plane needs to be defined in order to verify if the resist profile has resulted in resist top loss.

3. Implementation and Results

A 28 nm metal layer was used to demonstrate the 3D resist full chip verification flow and implementation for production, as this process has the most challenging low k1 factor with single patterning. For this technology, process window aware OPC had been used and optimized, but resist top loss hotspots still occurred as the OPC model had only been calibrated with wafer data at a single resist plane, and therefore was only designed to meet the target at a single resist plane.

Real time 3D resist compact simulation shows that different geometrical structures with the same dimensions at the resist bottom have resist profile degradation through positive and negative defocus, as shown in Figure 4.

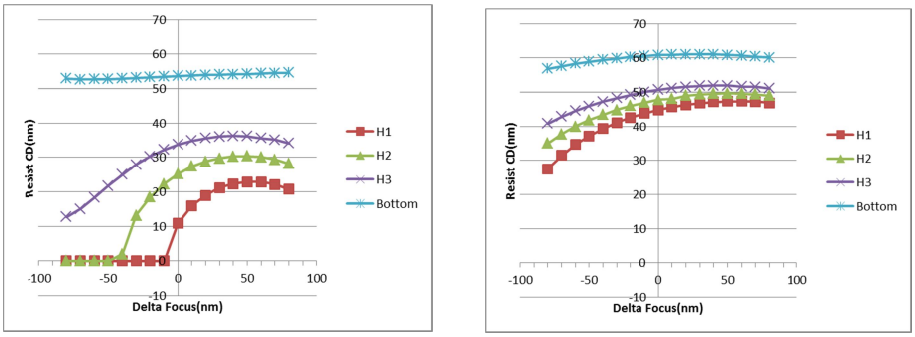

Figure 4 a) Pattern A using the 3D resist compact model simulation shows steep resist height degradation when focus varies; b) Pattern b using the 3D resist compact model simulation shows thinner resist at nominal focus condition, though focus degradation is less severe than for Pattern A. Bottom , H3, H2 and H1 represent different resist heights and Bottom > H3 > H2 > H1, bottom is where wafer CD collected for nominal model calibration.

The profile CD is estimated at different heights assuming optical effects dominate for the resist profile. Therefore, a resist profile degradation index(RPDI) is defined to estimate the severity of the impact of post litho resist profile degradation on post etch CDU changes.

RPDI = (bottom_CD – top_CD)/bottom_CD

A larger RPDI value means worse resist profile degradation which influences etch CDU more, with a maximum value of 1 meaning total resist top loss. Comparing RPDI values among weak points, between weak points and selected neighboring points where resist top CD loss was also relatively small is instructive.

Figure 5 shows a comparison of patterns that were chosen with relatively small resist top CD's around the weak points (called "warm points") to those with weak RPDI values.

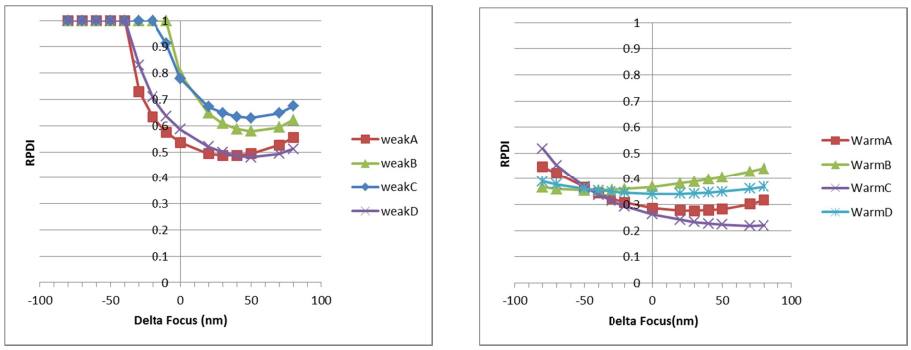

Figure 5 a) Severity of weak points is weak point A (weakA)>WeakD >WeakC >WeakB; b) Warm points shows less RPDI than real after etch weak points.

After checking the top resist shrinkage using the 3D resist compact model simulation on these hotspots through the process window and comparing to etch FEM wafer, a good correlation between RPDI and etch bridging defects through process window was found and a threshold was defined for a safe resist level which is the boundary for a good etch profile and stable etch CD uniformity and those that will cause a weak etch profile that is susceptible to process variation.

By implementing the 3D resist compact OPC model into full chip verification, a more robust OPC solution can be achieved not only for the lithography process, but also improving etch and CMP process stability. Figure 6 shows a good example of the 3D resist compact model implication. By regression of the OPC recipe with the full chip verification result using both resist bottom model and resist top model as the criteria, we significantly improved the full wafer manufacturing margin and extend the visibility of OPC verification from photo to etch and even CMP process. The process stability and yield reported show an impressive improvement.

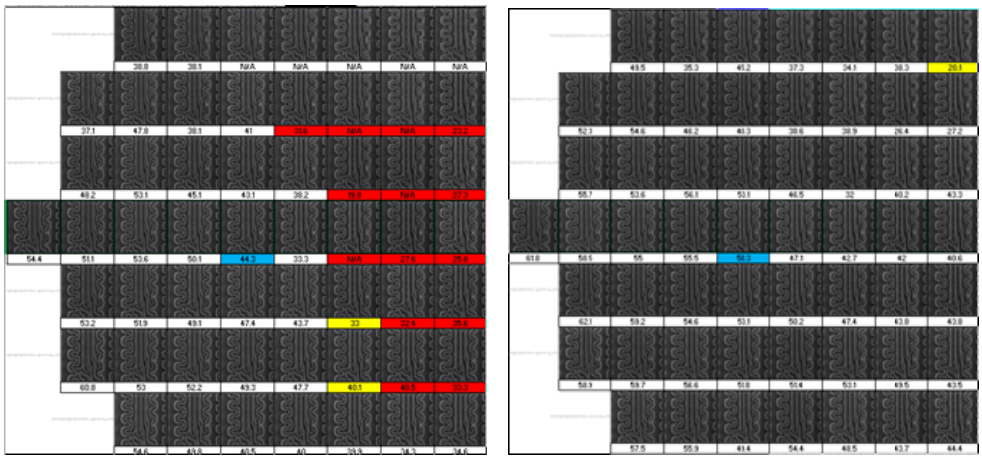

Figure 6 a) An OPC solution susceptible to resist top loss with a poor etch process margin; b) A better OPC solution that improves the etch process margin without scarifying the litho process.

In term of runtime, it is impractical to perform full chip simulation using a rigorous simulation tool. The compact 3D resist model is capable and effective for full chip simulation. Adding one compact 3D resist model at certain process conditions in full chip verification only induces a 15~20% runtime increase comparing to the original flow using only a resist bottom model. This is acceptable for mass production tape outs from a runtime point of view.

4. Conclusion

This paper demonstrated the concept of a 3D resist compact OPC model and its correlation with the litho and etch process. 3D resist full chip verification with 3D resist compact OPC model showed significant benefit for 28 nm metal layers with an OPC quality improvement. With a robust OPC solution, both litho and etch process can achieve larger process margins and more stable process capability. Yield improvement also proved the value of this methodology as an innovate solution for the challenges of low k1 lithography.

5. Future Work

Future studies will include a deeper exploration in to the relationship between the 3D resist profiles and inline yield and reliability hot spots with more efficient 3D simulation methods.

REFERENCES

[1] Xin Zheng, et al, “Resist loss in 3D compact modeling”, Proc. SPIE Vol. 8326, (2012).
[2] Bong-Soo Kang, et al, “Model-based searching method to find the integrated critical failure on the wafer”, SPIE Vol. 8327 (2012).